Lattice CrossLink-NX ISP Demo Quick Start Guide

Application Note

FPGA-AN-02040-1.0

September 2021

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults and associated risk the responsibility entirely of the Buyer. Buyer shall not rely on any data and performance specifications or parameters provided herein. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. No Lattice products should be used in conjunction with mission- or safety-critical or any other application in which the failure of Lattice's product could create a situation where personal injury, death, severe property or environmental damage may occur. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Contents

Figures

Tables

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AE	Auto Exposure
AWB	Auto White Balance
BLC	Black Level Correction
CCM	Color Correction Matrix
CFI	Color Filter Array Interpolation
DPC	Defective Pixel Correction
EVDK	Embedded Vision Development Kit
GAMMA	Gamma Correction
ISP	Image Signal Processing
TMAP	Tone Mapping
VIP	Video Interface Protocol

1. Overview

This document is intended to show you the hardware setup and operation procedures for demonstrating the Image Signal Processing (ISP) reference design features. It is assumed that you are familiar with the basic Lattice FPGA design flow.

This reference design is developed based on Lattice Embedded Vision Development Kit (EVDK) with CrossLink-NX VIP Sensor Input Board.

Lattice Embedded Vision Development Kit (EVDK) is comprised of (Figure 1.1):

- CrossLink-NX VIP Sensor Input Board
- ECP5 VIP Processor Board
- HDMI VIP Output Bridge Board

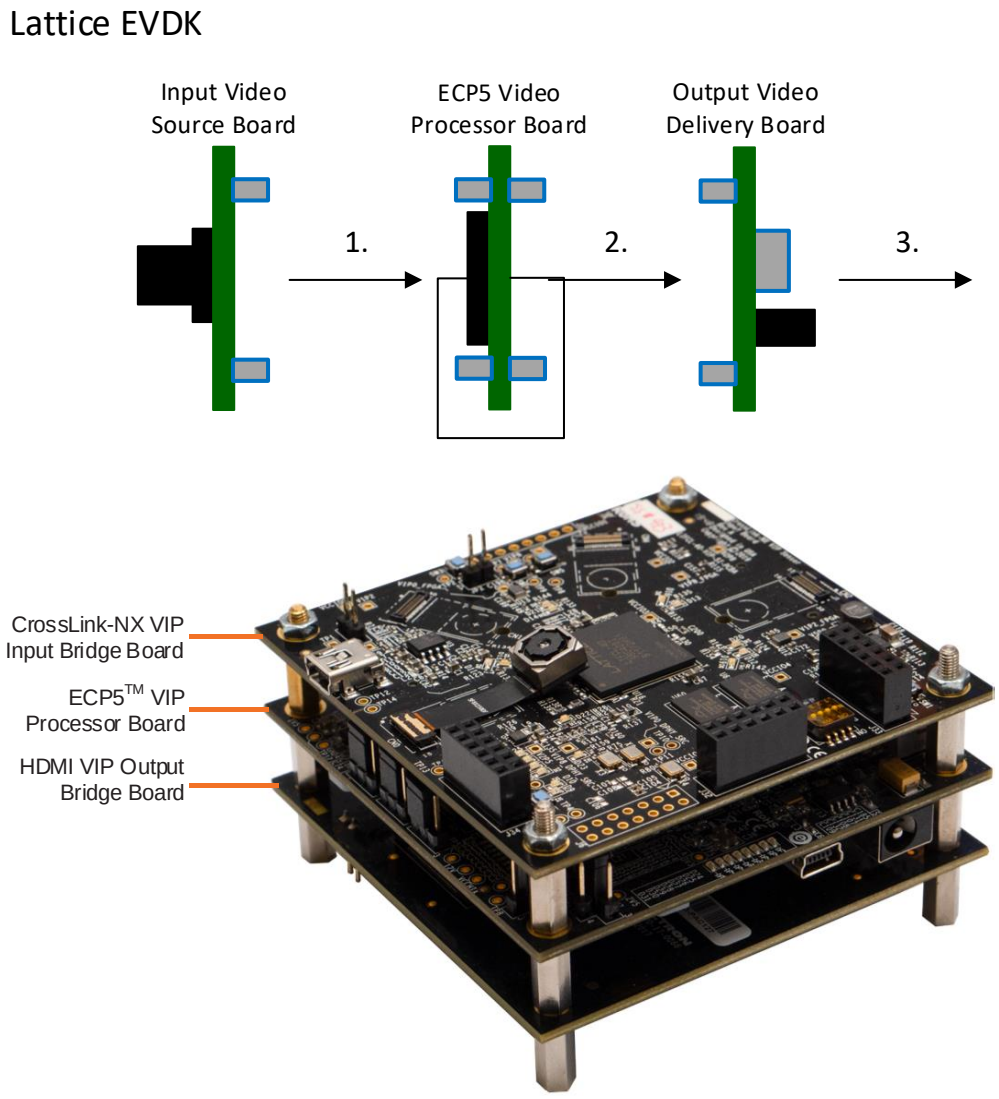

Figure 1.1. Lattice EVDK Components

For more details regarding Lattice EVDK, refer to Lattice Embedded Vision Development Kit User Guide (FPGA-UG-02015).

For more details regarding Lattice CrossLink-NX VIP Sensor Input Board, refer to CrossLink-NX VIP Sensor Input Board User Guide (FPGA-EB-02029).

2. ISP Reference Design Block Diagram

The ISP reference design captures sensor data, converts its interfaces, implements ISP pipelines, and finally displays the video on the HDMI monitor. Figure 2.1 shows the whole ISP reference design architecture and data flow.

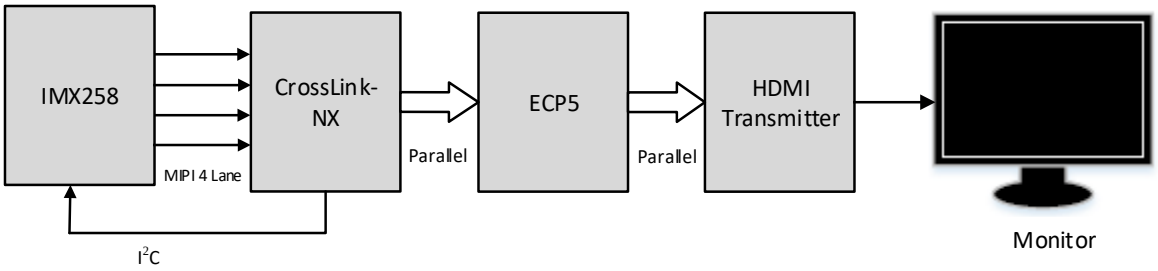

Figure 2.1. ISP Reference Design Architecture and Data Flow

The ISP core is implemented in the CrossLink-NX device. The CrossLink-NX device receives the MIPI sensor data, converts it to the parallel interface, implements ISP processing, and transmits the video to the HDMI transmitter. Figure 2.2 shows the Crosslink-NX ISP block diagram.

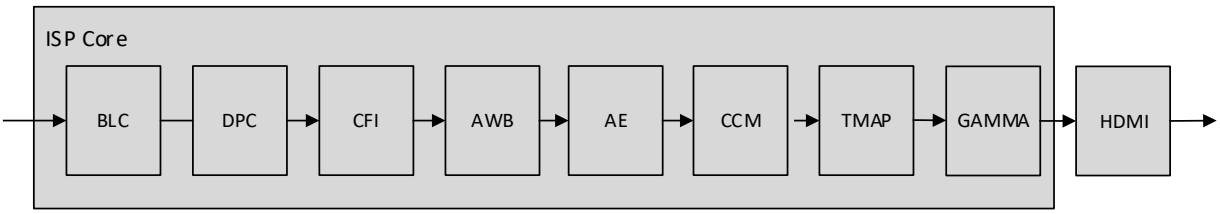

Figure 2.2. CrossLink-NX ISP Block Diagram

3. ISP Reference Design Jumper Settings

Following jumper settings for CrossLink-NX (Table 3.1) and ECP5 (Table 3.2) boards are required to enable the ISP function correctly.

Table 3.1. CrossLink-NX VIP Sensor Input Board Jumper Settings

Serial Number	Jumper Name	Status
1	JP2	Open
2	J3	Open
3	—	All other headers should be kept open.

Table 3.2. ECP5 VIP Input Bridge Board Jumper Settings

Serial Number	Jumper Name	Status
1	J55	Connect 1 and 2.
2	J51	Connect 1 and 2.
3	J5	Connect 1 and 2.
4	J9	Connect 1 and 2.
6	J6	Connect 1 and 2.
7	J3	Connect 1 and 2, also 5 and 6.
8	J50	Connect 1 and 2, also 3 and 5.
9	J7	Connect 2 and 3.
10	J52	Connect 1 and 2 for SPI 2, 2 and 3 for JTAG.
11	J53	Connect 1 and 2.
12	—	All other headers should be kept open.

4. ISP Reference Design Requirements

Following items are required for this reference design:

- LF-EVDK1-EVN
- CrossLink-NX VIP Sensor Input Board
- HDMI monitor
- HDMI cable
- DC power adapter (12 V)
- Laptop/PC
- Bit file
- USB 2.0 Type A to Mini-B cable*
- Lattice Diamond Programmer version 3.10 or higher*
- Lattice Radiant Programmer version 3.0 or higher*

*__Note__: Required only in the re-programming process.

5. Program CrossLink-NX/ECP5 Board

The following steps show you how to download the bitstream to CrossLink-NX/ECP5 board.

1. Connect the LF-EVDK1-EVN board to DC power adapter (12 V).
2. Connect the board to PC via USB mini port.
3. Start Radiant Programmer, Version 3.0 or a later version.
4. The Radiant Programmer — Getting Started dialog box pops up (Figure 5.1). By default, the *Create a new project from a scan* option is selected. Check and confirm other settings are correctly reflected the real components connected (Figure 5.1). Click OK, if everything is correct.

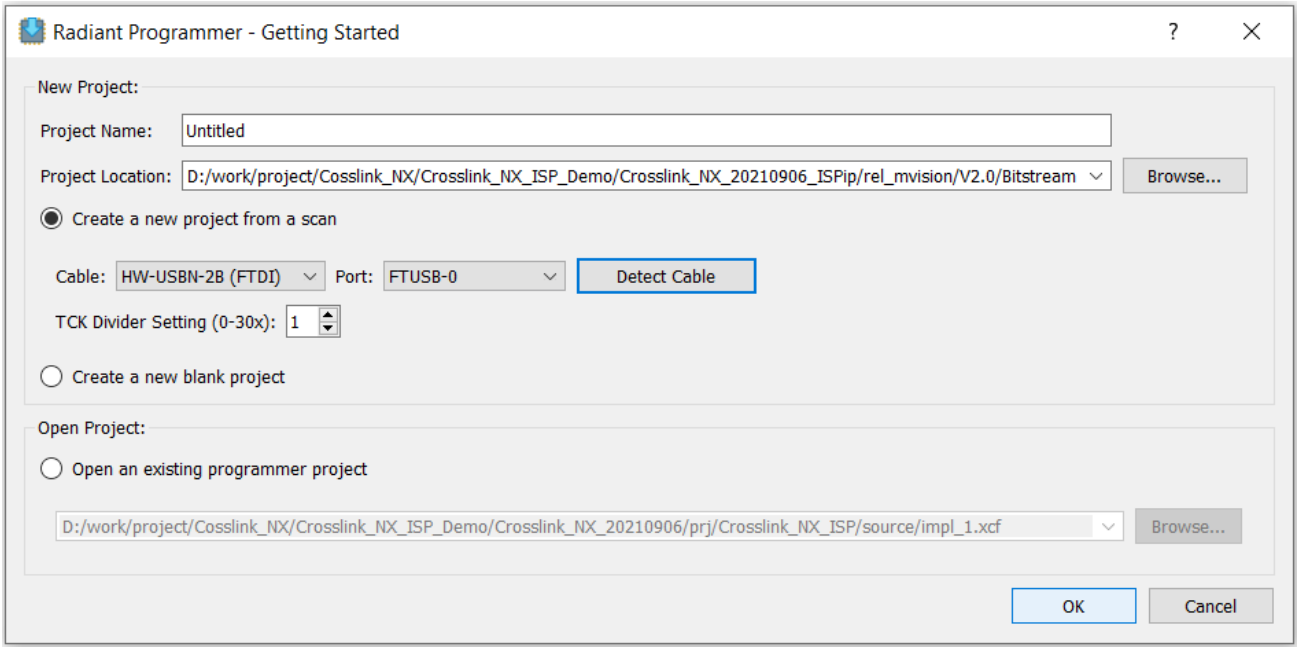

Figure 5.1. Getting Started dialog in Lattice Radiant Programmer

5. A new window pops up (Figure 5.2). Make sure the configuration settings for the CrossLink-NX Board are the same as those shown in Figure 5.2.

   Device Family: LIFCL

   Device: LIFCL-40

   Operation: Fast Program

   File Name: \\rel_mvision\V2.0\Bitstream\CrossLink-NX_ISP_impl_1.bit

   ...

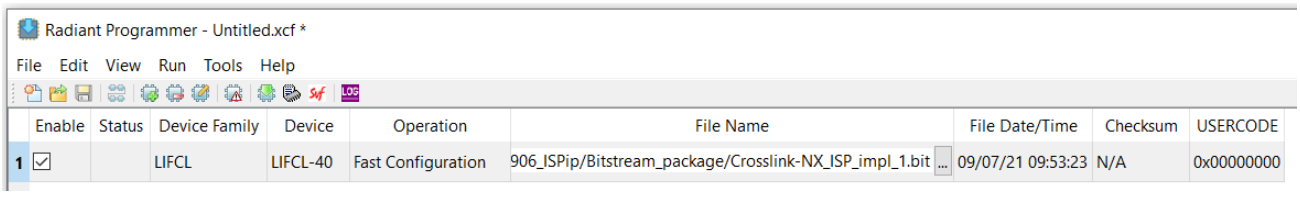

Figure 5.2. Set up Configuration Settings for CrossLink-NX Board

6. Click the Program Device icon  from the toolbar, or choose the **Design > Program** menu item from Radiant Programmer, to program the CrossLink-NX board. Check the programming status and result (Figure 5.3).

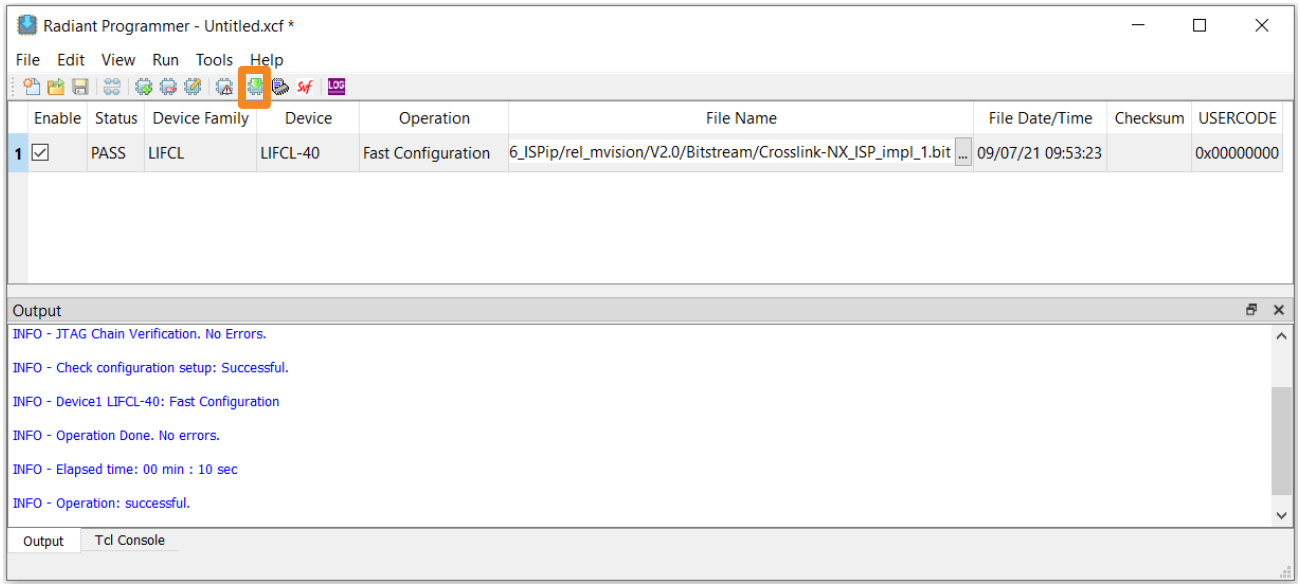

Figure 5.3 CrossLink-NX Board Programming Status and Result

7. Start Diamond Programmer, Version 3.10 or a later version. By default, the *Create a new project from a JTAG scan* option is selected. Check and confirm other settings are correctly reflected the real components connected (Figure 5.4). Click OK, if everything is correct.

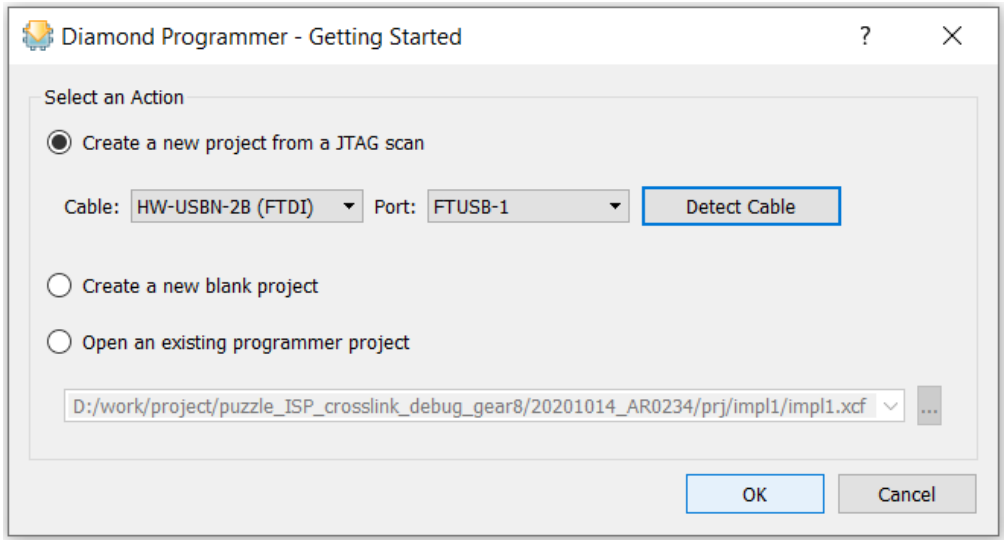

Figure 5.4 Getting Started dialog in Lattice Diamond Programmer

8. Make sure the configuration settings for the ECP5 Board are the same as those shown in Figure 5.5.

   Device Family: ECP5UM Device: LFE5UM-85F

   Operation: Fast Program

   File Name: \\rel_mvision\V2.0\Bitstream\ECP5_ISP_bridge_impl1.bit

   ...

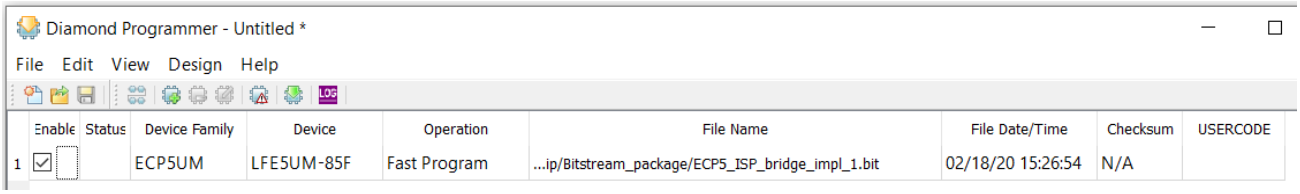

Figure 5.5. Set Up Configuration Settings for ECP5 Board

9. Click the Program icon  from the toolbar, or choose the **Design > Program** menu item from Diamond Programmer, to program the ECP5 board. Check the programming status and result (Figure 5.6).

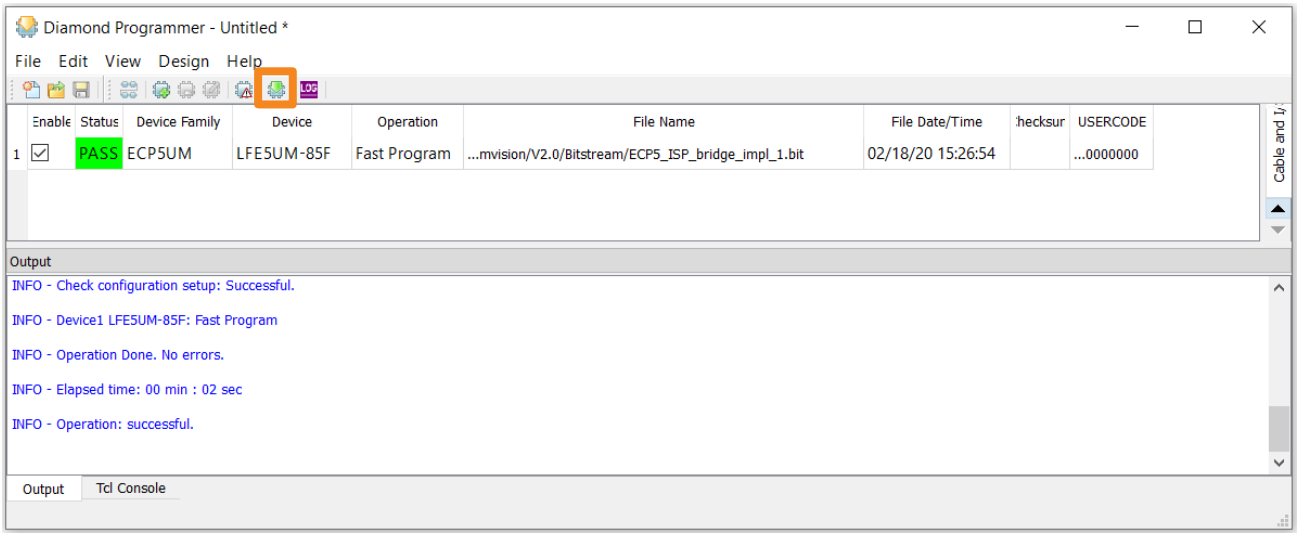

Figure 5.6. ECP5 Board Programming Status and Result

6. Display the Image Signal Processing Results

After programming the CrossLink-NX and the ECP5 boards successfully, follow the steps below to display the Image Signal Processing (ISP) results, the video of the camera, on the monitor.

1. Connect the HDMI monitor to the EVDK components via the HDMI cable.
2. Toggle the button “SW3 (SYS_RST)” on the CrossLink-NX VIP Sensor Input Board.
3. The video of the camera captured by the sensor can be displayed on the HDMI monitor.

7. Advanced Features and Tools

Besides those basic features of the ISP reference design discussed in the previous sections, some advanced features can also be accessed using SSP tools and running scripts.

7.1. Dynamic ISP Parameters Setup Using SSP Tools

Many registers are implemented in the ISP reference design to provide a dynamic way to control the logic and to setup ISP parameters. These registers can be accessed through the SSP tool.

Follow steps below to install and use the SSP tool in the ISP reference design.

1. Install the “mini-ssp” tool on PC.

   Double click <*Drive*>:\\rel_mvision\V2.0\Tools\LSCC_SSP.msi. The SSP tool can be installed on your PC.

   Once the tool is installed successfully, the following six documents can be found in <*Drive*>:\<install_folder>\<*Default_Company_Name*>\LSCC_SSP\doc\.

   - SSP Demo Quick Start.pdf
   - SSP Installation and Deployment Usage Guide.pdf
   - SSP Operation Tool Kits Usage Guide.pdf
   - SSP Register Mapping Interface Specifiction.pdf
   - SSP RTL Generator Usage Guide.pdf
   - SSP Simulation Platform Usage Guide.pdf

   Refer to these documents for the SSP tool usage accordingly.

2. Connect Lattice HW-USBN-2B cable with J34 of the CrossLink-NX VIP Sensor Input Board. Refer to Table 7.1 for the pin connection details between the HW-USBN-2B cable and J34.

Table 7.1. J34 and HW-USBN-2B Cable Pin Connection

J34 Number Pins on CrossLink-NX VIP Board	USBN-2B Cable
1	SCLK
2	SO
3	N/A
4	N/A
5	GND
6	VCC
7	SI
8	ISPEN
9	N/A
10	N/A
11	GND
12	VCC

3. After the configuration of the CrossLink-NX and ECP5 boards done, run RMI-based command to access registers. Four types of command are supported:

```
 rmi_write addr (16-bit Hex) data (32-bit Hex)
rmi_read addr (16-bit Hex) data_len (4x Decimal)
cam_write addr (16-bit Hex) data (several bytes Hex)
cam_read addr (16-bit Hex) data_len (Decimal)
```

Examples:

```
 rmi_write 0x0000 0x11223344
rmi_read 0x0000 4 (0x11223344 can be read out)
cam_write 0x0204 0x0128
  0x0204 is the sensor register address
  The command writes 0x01 => 0x0204,
     0x28 => 0x0205 into the sensor registers
     cam_read 0x0204 2 (0x0204/0x0205 sensor register values will be read out)
```

Refer to the file (\\rel_mvision\V2.0\DOC\mVision_ISP_register_map.xlsx) for the detailed register map table.

By configuring different registers, you can modify desired ISP parameters. After that, you can verify the configuration result by checking the image from the HDMI monitor.

References

- Lattice Embedded Vision Development Kit User Guide (FPGA-UG-02015)
- CrossLink-NX VIP Sensor Input Board User Guide (FPGA-EB-02029)

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.0, September 2021

Section	Change Summary
All	Production release.

www.latticesemi.com